IN THE CLAIMS

1. (currently amended) A universal clock generator comprising:

only one high frequency clock region having only one phase lock loop for generating high frequency clocks, the high frequency clock region being integrated in a first chip;

a low frequency clock region connecting to the high frequency clock region and integrated in a second ship, the low frequency clock region including:

(a) only one phase lock loop for generating low frequency clocks, and

(b) at least one delay lock loop for increasing a number of the high frequency clocks of the high frequency clock region; and

an oscillator connected to the low frequency clock region.

2. (canceled)

3. (original) The universal clock generator of Claim 1, wherein the low frequency clock region outputs a baseband clock acting as a reference frequency of the high frequency clock region.

4. (original) The universal clock generator of Claim 1, wherein output ends of the delay lock loop feedback to input ends of the delay lock loop for increasing a number of output clocks.

5. - 14. (canceled)

15. (previously presented) The universal clock generator comprising:

only one high frequency clock region for generating high frequency clocks, the high frequency clock region being integrated in a first chip;

a low frequency clock region connecting to the high frequency clock region and integrated in a second chip, the low frequency clock region including:

(a) only one phase lock loop for generating low frequency clocks; and

(b) at least one delay lock loop for increasing a number of the high frequency clocks of the high frequency clock region; and

an oscillator connected to the low frequency clock region.